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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,287	03/25/2004	Kenji Kamada	XA-10061	5093

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
LEE, CHUN KUAN	
ART UNIT	**PAPER NUMBER**
2181	

NOTIFICATION DATE	DELIVERY MODE
02/22/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ipdocketing@milesstockbridge.com
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Office Action Summary	Application No.	Applicant(s)	
	10/808,287	KAMADA ET AL.	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO ARGUMENTS

1. Applicant's arguments with respect to claims 1 and 3-5 have been considered but are moot in view of the new ground(s) of rejection. Currently, claim 2 is canceled and claims 1 and 3-5 are pending for examination.

2. In response to applicant's arguments, on page 5, 3rd paragraph, regarding the amended independent claim 1 rejected under 35 U.S.C. 103(a) that the combination of references does not teach/suggest the amended claimed limitation of "... a first memory external to the direct memory access controller ..."; applicant's arguments have fully been considered, but are not found to be persuasive.

Please note that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The examiner relied on Farazmandnia for the teaching of the above amended claimed limitation, wherein Farazmandnia teaches a first memory (Fig. 2, ref. 204) is external to a direct memory access controller (Fig. 2, ref. 206).

II. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laine et al. (US Patent 6,687,796) in view of Farazmandnia et al. (US Patent 6,728,795).

4. As per claim 1, Laine teaches a serial communication device, comprising:

a serial interface (e.g. serial port) to receive data (col. 7, l. 66 to col. 8, l. 7); and

a direct memory access (DMA) controller (Fig. 2-3B, ref. 210) to transfer said data received by said serial interface from said serial interface to a first memory (e.g. first-in first-out (FIFO) buffer) (col. 5, ll. 36-54),

wherein said DMA controller is started up before said serial interface receives said data (col. 6, ll. 20-24), as the DMA controller's port must be able to respond to the received request for data transferring, the DMA controller must be already active (i.e. already started up) before receiving the request;

said DMA controller (Fig. 2, ref. 210) sets a number of transfers before said serial interface receives said data (col. 5, l. 19 to col. 6, l. 24), wherein the number of transfers is set by the DMA controller via the DMA controller setting by configuring the size of the FIFO,

the number of data received (e.g. received by reading) at a time by the serial interface (e.g. serial port) (col. 5, l. 19 to col. 6, l. 24 and col. 7, l. 66 to col. 8, l. 7), and

said direct memory access controller (Fig. 3A, ref. 370) outputs a direct memory access transfer end interrupt signal to a central processing unit (e.g. CPU) (col. 6, ll. 62-64), as the interrupt generator (Fig. 3A, ref. 370) generating interrupts to the CPU according to the DMA configuration and state.

Laine does not teach the serial communication device, comprising:

wherein the first memory is external to the direct memory access controller;

setting a number larger than the number of data received ...; and

the number of data transferred from said serial interface ... .

Farazmandnia teaches a system and a method comprising:

a first memory (Fig. 2, ref. 204) is external to a direct memory access controller (Fig. 2, ref. 206);

setting a number (e.g. number set to 7 as the DMA FIFO have 7 blocks for data buffering) larger than the number of data received at a time (e.g. one byte is received at a time) as the number of transfers to said first memory (e.g. DMA FIFO 204 of Fig. 2) (col. 1, l. 52 to col. 2, l. 17), as the DMA FIFO is preferably set to a size of 8 bytes, with 7 blocks have one byte each for buffering data, which is larger than the number of one byte data that is received at a time, as a number of transfers; and

the number of data transferred from a serial interface (Fig. 2, ref. 200) to the first memory (e.g. DMA FIFO 204 of Fig. 2) reaches said number set as the number of

transfers (col. 1, l. 52 to col. 2, l. 17), wherein the number data transferred reaches the number of transfers as the DMA FIFO is filled.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Farazmandnia's transferring of data when the FIFO is filled into Laine's DMA controller for the benefit of providing a high-speed asynchronous data transferring (Farazmandnia, col. 1, ll. 52-55) to obtain the invention as specified in claim 1.

5. As per claim 3, Laine and Farazmandnia teach all the limitations of claim 1 as discussed above, where Farazmandnia further teaches the serial communication device comprising wherein said serial interface outputs a receive timeout interrupt signal to said central processing unit when said data reception is stopped for a certain period after the start of said data reception (Farazmandnia, col. 2, ll. 1-17), wherein the transferring of data from the FIFO buffer to the host memory is resulted from a timer expiring, which would also initiate the corresponding transferring of interrupt to the CPU.

6. As per claim 4, Laine and Farazmandnia teach all the limitations of claim 3 as discussed above, where Farazmandnia further teaches the serial communication device comprising wherein said direct memory access controller retransfers said transferred data from said first memory (Farazmandnia, DMA buffer 204 of Fig. 2) to a second memory (Farazmandnia, host memory 208 of Fig. 2) as triggered by said direct memory

access transfer end interrupt signal or said receive timeout interrupt signal (Farazmandnia, col. 1, l. 52 to col. 2, l. 17).

7. As per claim 5, Laine and Farazmandnia teach all the limitations of claim 1 as discussed above, where both further teach the serial communication device comprising

wherein said first memory is comprised of two or more memory areas (Laine, FIFO 0, FIFO 1, FIFO 2, FIFO 3, FIFO 4, FIFO 5 of Fig. 3A), and

wherein said direct memory access controller has a continuous transfer function and transfers said data from said serial interface to said first memory while alternately switching the destinations of the data received by said serial interface among said two or more memory areas as triggered by said direct memory access transfer end interrupt signal or a receive timeout interrupt signal (Laine, col. 16, ll. 49-57 and Farazmandnia, col. 1, l. 52 to col. 2, l. 17), wherein the DMA controller is a multi-channel DMA controller and servicing each corresponding channels in a round-robin method, therefore, in finishing the servicing of one of the channels, the multi-channel DMA controller switches to receiving data for the next channel into the corresponding FIFO buffer, wherein the servicing finished either from the filling of the FIFO buffer or the expiration of the timer.

III. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, claims 1 and 3-5 have received a final action on the merits. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

February 06, 2008

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

ALFORD KINDRED
SUPERVISORY PATENT EXAMINER